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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,922	08/17/2006	Edwin Jan Van Dalen	NL04 0159 US1	3764

65913 7590 05/26/2010

NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
CRUTCHFIELD, CHRISTOPHER M	

ART UNIT	PAPER NUMBER
2466	

NOTIFICATION DATE	DELIVERY MODE
05/26/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 10/589,922	Applicant(s) VAN DALEN ET AL.	
	Examiner Christopher Crutchfield	Art Unit 2466	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8 and 9* is/are rejected.

7)☒ Claim(s) *6-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

   1. Determining the scope and contents of the prior art.
   2. Ascertaining the differences between the prior art and the claims at issue.
   3. Resolving the level of ordinary skill in the pertinent art.
   4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. **Claims 1, 2, 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Srikanteswara*, et al. (S. Srikanteswara, J. Reed, P. Athanas, R. Boyle, A Soft Radio Architecture for Reconfigurable Platforms, IEEE Communications Magazine, Feb. 2000, Pages

140-147) in view of *Marinissen I*, et al. (E. Marinissen I , Y. Zorian , R. Kapur , T. Taylor and L. Whetsel, Towards a Standard for Embedded Core Test: An Example, Proceedings of the IEEE International Test Conference, Pages 616-627, 1999) and *Marinissen II*, et al. (E. Marinissen, R. Kapur, M. Lousberg, T. McLaurin, M. Ricchetti and Y. Zorian, On IEEE P1500's Standard for Embedded Core Test, Journal of Electronic Testing, Springer Netherlands, Issue Volume 18, Numbers 4-5 / August, 2002, Pages 365-383).

Regarding claim 1, *Srikanteswara* discloses an electronic signal processing circuit, comprising:

a. A plurality of chained stream processing circuits, each having a stream input and a stream output, for inputting and outputting an input and output stream of successive sample values (Pages 142-147). (The system of *Srikanteswara* discloses a stream based processing architecture for software radios [Pages 142-143]. The architecture operates by programming individual processing elements [i.e. stream processing circuits] to perform discrete functions for the software radio [See Figs. 1 and 2, and Pages 143-144, "The Processing Layer]. The processing element I/O's are linked by a bus [i.e. the linking circuit] which feeds the stream of sampled data from, for example, the A/D converter [See Fig. 1, “Data from A/D Converter”] through the processing elements where the desired functions are performed on the data [See, for example, Pages 144-147, “Implementation of an Adaptive Single User CDMA Receiver” - Showing the stream processing for a CDMA Receiver].)

b. Linking circuits, each linking a respective pair of stream processing circuits, each linking in a normal mode, the linking circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair (Pages 142-147 - See (a), Supra).

Srikanteswara fails to disclose the use of test access points for each of the streamed processing circuits to allow for test access to the inputs and outputs of the stream processing circuits such that the system further comprises linking multiplexing circuits, each linking a respective pair of stream processing circuits, each linking multiplexing circuit being individually switchable to a normal mode and to a replacement mode, the linking multiplexing circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair and the system further comprises a shareable communication structure coupled to the linking multiplexing circuits, each linking multiplexing circuit, when in the replacement mode, providing a continuous connection for supplying successive sample values from a second stream from the communication structure to a receiving one of the stream processing circuits in the respective pair of the linking multiplexing circuit and a control circuit coupled to the linking multiplexing circuits, arranged to keep a selectable one of the multiplexing circuits in the replacement mode so that the selectable one of the linking multiplexing circuits passes a stream of successive sample from the second stream to the receiving one of the processing circuits in the respective pair of linking multiplexing circuit, while keeping at least part of the other linking multiplexing circuits in the normal mode.

In the same field of endeavor, *Marinissen I* discloses the use of test access points for each of the streamed processing circuits to allow for test access to the inputs and outputs of the stream processing circuits such that the system further comprises:

a. Linking multiplexing circuits, each linking a respective pair of stream processing circuits, each linking multiplexing circuit being individually switchable to a normal mode and to a replacement mode, the linking multiplexing circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair and a shareable communication structure coupled to the linking multiplexing circuits, each linking multiplexing circuit, when in the replacement mode, providing a continuous connection for supplying successive sample values from a second stream from the communication structure to a receiving one of the stream processing circuits in the respective pair of the linking multiplexing circuit (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to

the inputs of the cores when the core is in the serial internal test mode [i.e. replacement mode] [See Fig. 8(d)].)

c. A control circuit coupled to the linking multiplexing circuits, arranged to keep a selectable one of the multiplexing circuits in the replacement mode so that the selectable one of the linking multiplexing circuits passes a stream of successive sample from the second stream to the receiving one of the processing circuits in the respective pair of linking multiplexing circuit (Page 621, Fig. 3 and Pages 625-626, Figs 7, 8 and Table 3). (The system of *Marinissen I* discloses that the control circuit sets the mode of the linking multiplexing circuit via the WC connections [Page 621, Fig. 3], which control the connections of the wrapper input cell multiplexer to set the mode of the core [See Pages 625-626, Fig. 7(b), Figs 8(a) and (d) and Table 3]. When one of the link multiplexing circuit is set in the internal test mode, samples form the second stream/test rail are passed into the core/processor via the “wci” multiplexer [Pages 625-626, Fig. 7(b) and Table 3].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided

by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

Marinissen I fails to disclose that the control circuit keeps a selectable one of the multiplexing circuits in the replacement mode while keeping at least part of the other linking multiplexing circuits in the normal mode. In the same field of endeavor, *Marinissen II* discloses that the control circuit keeps a selectable one of the multiplexing circuits in the replacement mode while keeping at least part of the other linking multiplexing circuits in the normal mode (Pages 378-381, Figs. 11(a) and 11(b), Table 2 and the Last Paragraph of Page 378, carried onto Page 381). (The system of *Marinissen II* discloses the fact that the cores/stream processors in the normal and bypass modes have non-conflicting inputs to the multiplexers [i.e. as shown in table 2, the set bits in the normal mode correspond to the dont care bits in the bypass mode and vice versa]. Therefore, the system of *Marinissen II* collapses the Bypass and the Normal mode into a single mode [See The Last Paragraph of Page 378, carried onto Page 381]. The result of this operation is that when all of the cores except the core under test [which is placed into the replacement or serial internal test mode] are placed into the bypass mode [as suggested by both *Marinissen I* and *Marinissen II*] the cores are also in the normal functional mode. The same technique can also be applied to *Marinissen I* which has a similar arrangement of don't care bits in the normal and serial bypass modes [See *Marinissen I*, Page 626, Table 3].)

Therefore, since *Marinissen II* suggests collapsing the bypass and normal operating modes into a single mode, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the collapsed modes of *Marinissen II* into the teachings of *Srikanteswara* as modified by *Marinissen I* by collapsing the control inputs for setting the normal and bypass mode into a single set of inputs. The motive to combine is to reduce the instruction set size of the wrapper instruction register.

Regarding claim 2, *Srikanteswara* fails to disclose an electronic signal processing circuit comprising interface circuits, each coupled between the communication structure and the stream output of a respective one of the stream processing circuits, each interface circuits being individually switchable to an output mode under control of the control circuit (IS), each interface circuit, when in the output mode, passing successive samples of the second stream or a further stream from the stream output of a respective one of the stream processing circuits to the communication structure. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing circuit comprising interface circuits, each coupled between the communication structure and the stream output of a respective one of the stream processing circuits, each interface circuits being individually switchable to an output mode under control of the control circuit (IS), each interface circuit, when in the output mode, passing successive samples of the second stream or a further stream from the stream output of a respective one of the stream processing circuits to the communication structure (Pages 289, Fig. 5 and 292, Fig. 10(a)). (The system of *Marinissen I* further discloses that in addition to inserting samples at the input ports of the cores/stream processors via the linking multiplexer, the system may also capture the output of each of the cores/stream processors made in response to an input test stream [i.e. the "second stream"] inserted from the serial TestRail [i.e. communications structure] by using a multiplexer [i.e. interface circuit] [See Page 625, Fig. 7(c), The multiplexer controlled by the "wco" input] attached to the output of the core and may re-direct the core output to the system TestRail [i.e. communications structure] [See Pages 625-262, Fig. 8(d), Fig. 7(c) and Table 3].)

Therefore, since *Marinissen I* suggests the use of output re-direction of test streams for core testing, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the output re-direction of *Marinissen I* with the stream processors of *Srikanteswara* by using the TestRail/communications structure and the link multiplexing circuit

to introduce a test/second stream to the input of a core/stream processor to be tested, and to then use the interface circuit/output multiplexer to capture the result of the test and re-direct the test output to the TestRail/communication structure. The motive to combine is to allow observance of the response of cores to a particular input, thereby allowing the testing and observation of internal cores.

Regarding claim 8, *Srikanteswara* fails to disclose an electronic signal processing circuit comprised on an integrated circuit chip. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing circuit comprised on an integrated circuit chip (Pages 616-617). Therefore, since *Marinissen I* suggests placing multiple core processors on a single integrated circuit, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the chained streamed processors and the electronic signal circuit of *Srikanteswara* on a single IC. The motive to combine is to reduce costs by using a single IC to perform all the required tasks.

Regarding claim 9, *Srikanteswara* discloses a plurality of stream processing circuits that are connected in a network which passes streams of sample values between pairs of the stream processing circuits (Pages 142-147). (The system of *Srikanteswara* discloses a stream based processing architecture for software radios [Pages 142-143]. The architecture operates by programming individual processing elements [i.e. stream processing circuits] to perform discrete functions for the software radio [See Figs. 1 and 2, and Pages 143-144, "The Processing Layer”]. The processing element I/O's are linked by a bus [i.e. the linking circuit] which feeds the stream of sampled data from, for example, the A/D converter [See Fig. 1, “Data from A/D Converter] through the processing elements where the desired functions are performed on the data [See, for example, Pages 144-147, “Implementation of an Adaptive Single User CDMA Receiver” - Showing the stream processing for a CDMA Receiver].)

Srikanteswara fails to disclose a method further comprising an electronic signal processing circuit that comprises a plurality of stream processing circuits that are connected in a network which passes streams of sample values between pairs of the stream processing circuits, the method comprising providing a shareable communication structure coupled to stream inputs and outputs of the stream processing circuits, the shareable communication structure being redundant during normal use of the electronic signal processing circuit and in a test mode, extracting output streams from selected normally internal stream processing circuits or supplying input streams to selected normally internal stream processing circuits via the shareable communication structure. In the same field of endeavor, *Marinissen I* discloses a method further comprising an electronic signal processing circuit a that comprises a plurality of stream processing circuits that are connected in a network which passes streams of sample values between pairs of the stream processing circuits, the method comprising providing a shareable communication structure coupled to stream inputs and outputs of the stream processing circuits, the shareable communication structure being redundant during normal use of the electronic signal processing circuit and in a test mode, extracting output streams from selected normally internal stream processing circuits or supplying input streams to selected normally internal stream processing circuits via the shareable communication structure (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing

the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores when the core is in the serial internal test mode [i.e. replacement mode] [See Fig. 8(d)]. The serial test rail is redundant and is not used for communication between the cores when the system is operating in normal mode [See Fig. 8(a)].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

5. **Claims 3-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Srikanteswara*, et al. (S. Srikanteswara, J. Reed, P. Athanas, R. Boyle, A Soft Radio Architecture for Reconfigurable Platforms, IEEE Communications Magazine, Feb. 2000, Pages 140-147) in view of *Marinissen I*, et al. (E. Marinissen I , Y. Zorian , R. Kapur , T. Taylor and L. Whetsel, Towards a Standard for Embedded Core Test: An Example, Proceedings of the IEEE International Test Conference, Pages 616-627, 1999) and *Marinissen II*, et al. (E. Marinissen, R.

Kapur, M. Lousberg, T. McLaurin, M. Ricchetti and Y. Zorian, On IEEE P1500's Standard for Embedded Core Test, Journal of Electronic Testing, Springer Netherlands, Issue Volume 18, Numbers 4-5, August, 2002, Pages 365-383) as applied to claim 2 and further in view of *Zorian*, et al. (Y. Zorian, E. Marinissen I, S. Dey, Testing Embedded-Core Based System Chips, Proceedings of the IEEE International Test Conference, 1998, Pages 130-143).

Regarding claim 3, *Srikanteswara* fails to disclose an electronic signal processing circuit according wherein the communication structure comprises a plurality of chained multiplexing circuits, individually controllable by the control circuit, each chained multiplexing circuit corresponding to a respective corresponding one of the stream processing circuits, each having a first input, a second input and an output, the first input being coupled to the stream output of the corresponding one of the stream processing circuits, the second input being coupled to the output of the chained multiplexing circuit a preceding one of the stream processors. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing circuit according wherein the communication structure comprises a plurality of chained multiplexing circuits, individually controllable by the control circuit, each chained multiplexing circuit corresponding to a respective corresponding one of the stream processing circuits, each having a first input, a second input and an output, the first input being coupled to the stream output of the corresponding one of the stream processing circuits, the second input being coupled to the output of the chained multiplexing circuit of a preceding one of the stream processors (Figs. 7 and 8). (The system of *Marinissen I* discloses the use of a bypass circuit connected to a multiplexer [i.e. the chained multiplexing circuit] [See Fig. 7(a), “Bypass” and the “m5” multiplexer]. The chained multiplexing circuit is connected to two inputs. The first is the connected to the output of the associated stream processing circuit [See Fig. 5(a), "M6" the

upper connection to the outputs of core A][i.e. the stream output of the corresponding stream processing circuit]. The second is connected to the previous core/chain processor via the serial TestRail/shareable communication structure [See Fig. 7(a), "si", “bypass”, "m6” - Showing the lower connection to the chain multiplexer connected to the so output of the previous core], which is in turn connected to the output of the previous core's/processor’s chained multiplexing circuit [See Fig. 7(a), “so”].)

Therefore, since *Marinissen I* suggests the use of a chained multiplexer to allow a bypass mode for the serial TestRail, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the bypass and chained multiplexer of *Marinissen I* into the teachings of *Srikanteswara* by inserting a bypass register and chained multiplexer into the shareable communications structure of *Srikanteswara* as modified by *Marinissen I*. The motive to combine is provided by is to reduce the time necessary to access each of the cores by allowing the bypassing of cores not involved in the present testing.

Srikanteswara as modified by *Marinissen I* fails to disclose an electronic signal processing circuit wherein the communication structure further comprises a plurality of chained multiplexing circuits wherein the second input is coupled to the output of the chained multiplexing circuit that corresponds to a preceding one of the stream processing circuit whose stream output is linked to the corresponding one of the stream processing circuit by one of the multiplexing circuits (i.e. *Marinissen I* fails to disclose that the connection order of the TestRail chains via the chained multiplexers coincides with the order of the input-output flow of data through the chained processors). In the same field of endeavor, *Zorian* discloses a plurality of chained multiplexing circuits wherein the second input is coupled to the output of the chained multiplexing circuit that corresponds to a preceding one of the stream processing circuit whose stream output is linked to the corresponding one of the stream processing circuit by one of the

multiplexing circuits (Figs. 5 and 6 and Pages 135-136, Section 6). (*Zorian* discloses a series of cores/processors which are linked up to form a chain in which the outputs of each core are connected to the inputs of the next core [See Fig. 6, Connections between Cores A, B and C]. *Zorian* further discloses that the test rail/communications structure connection via the chained multiplexing circuits may follow a path that coincides with the chained flow of the input-output ports of the processors [See Fig. 5, the TestRail connection that is connected through cores A, B and C].)

Therefore, since *Zorian* suggests the use of a TestRail flow via chained multiplexers that matches the direction flow of inputs and outputs through a series of chained processors, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the system of *Zorian* with the teachings of *Srikanteswara* as modified by *Marinissen I* by connecting the test rail and chained multiplexer connections in the same direction as the flow of data through the chained processors. The motive to combine is to make the ordering of the processors/cores on the TestRail connection easier to comprehend by ordering the TestRail connections in the same direction and order as the flow of data through the cores and to allow rapid testing of the interconnections between the processors (i.e. if the order of the flow of data over the TestRail did not match the order of the flow of data through the interconnections through the chained cores, it would not be possible to directly test all the interconnects between each of the cores using a serial test bus by continuously providing input data at the output of an upstream core associated with a link to be tested and continuously capturing the data on the other side of the connection at the input of the downstream core because the input test stream and the output result stream would “cross” on the serial TestRail for some subset of the directly connected cores and would have to be multiplexed, reducing speed and requiring additional data capture circuitry.)

Regarding claim 4, *Srikanteswara* fails to disclose an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores from the chained multiplexing circuit [See Fig. 7(b) - from chip]. The test values [i.e. samples of the second stream] are supplied from the core’s chained multiplexing circuit, which receives the values via its second input from the previous core’s chain multiplexing circuit [See Fig. 7, “m6”, “si” and “so”] [See Also claim 3, Supra].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail containing the chained multiplexing circuits linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail using chained multiplexing circuits and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

Regarding claim 5, *Srikanteswara* fails to disclose an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a

multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores from the chained multiplexing circuit [See Fig. 7(b) - from chip]. The test values [i.e. samples of the second stream] are supplied from the core’s chained multiplexing circuit, which receives the values via its second input from the previous core’s chain multiplexing circuit [See Fig. 7, “m6”, “si” and “so”] [See Also claim 3, Supra].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail containing the chained multiplexing circuits linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail using chained multiplexing circuits and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

Srikanteswara as modified by *Marinissen I* fails to disclose an electronic signal processing circuit wherein each linking multiplexing circuit further comprises a second input

receiving the second stream which is supplied to the second input of the chained multiplexing circuit that corresponds to the preceding one of the stream processing circuits whose stream output is linked to the input of the linked one of the stream processing circuits (i.e. *Marinissen I* fails to disclose that the connection order of the TestRail chains via the chained multiplexers coincides with the order of the input-output flow of data through the chained processors). In the same field of endeavor, *Zorian* discloses a plurality of chained multiplexing circuits wherein the second input is coupled to the output of the chained multiplexing circuit that corresponds to a preceding one of the stream processing circuit whose stream output is linked to the corresponding one of the stream processing circuit by one of the multiplexing circuits (Figs. 5 and 6 and Pages 135-136, Section 6). (*Zorian* discloses a series of cores/processors which are linked up to form a chain in which the inputs of each core are connected to the outputs of the next core [See Fig. 6, Connections between Cores A, B and C]. *Zorian* further discloses that the test rail/communications structure connection via the chained multiplexing circuits may follow a path that coincides with the chained flow of the input-output ports of the processors [See Fig. 5, the TestRail connection that is connected through cores A, B and C].)

Therefore, since *Zorian* suggests the use of a TestRail flow via chained multiplexers that matches the direction flow of inputs and outputs through a series of chained processors, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the system of *Zorian* with the teachings of *Srikanteswara* as modified by *Marinissen I* by connecting the test rail and chained multiplexer connections in the same direction as the flow of data through the chained processors. The motive to combine is to make the ordering of the processors/cores on the TestRail connection easier to comprehend by ordering the TestRail connections in the same direction and order as the flow of data through the cores and to allow rapid testing of the interconnections between the processors (i.e. if the order of the flow of data

over the TestRail did not match the order of the flow of data through the interconnections through the chained cores, it would not be possible to directly test all the interconnects between each of the cores using a serial test bus by continuously providing input data at the output of an upstream core associated with a link to be tested and continuously capturing the data on the other side of the connection at the input of the downstream core because the input test stream and the output result stream would “cross” on the serial TestRail for some subset of the directly connected cores and would have to be multiplexed, reducing speed and requiring additional data capture circuitry.)

Allowable Subject Matter

6. **Claims 6 and 7** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter. The prior art does not disclose the use of a second shareable communications structure for linking a second set of chain processors to a router having a first, second and third input coupled to an output of the shareable communication structure, an output of the further shareable communication structure and a first external connection terminal of the electronic signal processing circuit respectively, the router circuit having a first, second and third output, coupled to an input of the shareable communication structure, an input of the further shareable communication structure and a second external connection terminal of the electronic signal processing circuit respectively, the router circuit being arranged to establish selectable

connection patterns between its inputs and outputs under control of the control circuit as required by claims 6 and 7. That is, the closest prior art concerning the use of chained processors, *Srikanteswara,* does not disclose the use of a second set of chained processing circuits that is connected with a router circuit arranged to establish a selectable connection pattern between the inputs and the outputs of the first and second set of chain processors. Although one could argue that *Srikanteswara* suggests the use of a first and second set of chained stream processors in the form of a chained transmitter and receiver, it still does not suggest the use of a router between the two. Other art, for example, *Heutmaker*, et al. (US Patent No. 5,481,186) could arguably bridge this gap by demonstrating a loop back test that uses a “router” that loops back the output of a transmitter into the receiver [See Fig. 2], but it still provides no guidance as to why the router requires three inputs and outputs or why a separate set of link multiplexing circuits with a separate further shareable communication structure would be required for testing purposes when the same scan chain/TestRail may serve both transmitter and receiver. Therefore, given the number and type of modifications already used to reject independent claim 2, further modifying the claim with several additional references to arrive at the disclosure of claim 6 is beyond the skill of a person of ordinary skill in the art.

Prior Art Made of Record

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. *Whetsel*, et al. (US Patent No. 6,260165 B1) - Showing the testing of circuits contained within an IC using a linked input-output chain (See Fig. 7).

b. *Li*, et al. (J. Li, H. Huang, J. Chen, C. Su, C. Wu, C. Cheng, S. Chen, C. Hwang, H. Lin, A Hierarchical Test Methodology for Systems on Chip, IEEE Micro, Vol. 22, Issue 5, Sept 2002, Pages 69-81) - Outlining the IEEE 1500 and other SoC testing methods.

c. *Oakland*, et al. (S. Oakland, Considerations for Implementing IEEE 1149.1 on System-on-a-Chip Integrated Circuits, Proceedings of the 2000 IEEE International Test Conference, Pages 628-637) - Showing another chained SoC test mechanism.

d. *Song*, et al. (J. Son, S. Park, A Simple Wrapped Core Linking Module for SoC Test Access, Proceedings of the 11th Asian Test Symposium, Pages 344-350, 2002) - Showing a SoC chained test mechanism.

e. *Mitola*, et al. (J. Mitola, Software Radio Architecture: A Mathematical Perspective, IEEE Journal on Selected Areas in Communications, Vol. 17, No. 4, April 1999, Pages 514-538) - Showing the software layout of a stream based processing system for a software radio.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Crutchfield whose telephone number is (571) 270-3989. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel Ryman can be reached on (571) 272-3152. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher Crutchfield/
Examiner, Art Unit 2466
5/19/2010

/Daniel J. Ryman/
Supervisory Patent Examiner, Art Unit 2466